IN THE CLAIMS:

The status of each claim that has been introduced in the above-referenced application is identified in the ensuing listing of the claims. This listing of the claims replaces all previously submitted claims listings.

1. (Currently amended) A method ~~of~~ for forming an isolation structure for a semiconductor device, comprising:

~~providing a layered structure comprising~~ depositing a dielectric material onto a semiconductor substrate;

depositing ~~, a dielectric layer, and~~ a buffer ~~film layer~~material onto the dielectric material;

removing a portion of the buffer film material, a portion of the dielectric material, and material from the semiconductor substrate to form at least one trench extending into the semiconductor substrate, the trench including at least one side wall that lacks recesses;

~~etching said layered structure through said buffer film layer, through said dielectric layer, and into said semiconductor substrate to define a trench having sidewalls and a bottom;~~

forming an oxide ~~layer~~ on exposed portions of ~~said~~ the semiconductor substrate within ~~said~~ the trench;

~~selectively etching a portion of said~~ removing a portion of the buffer ~~film layer~~ material to laterally recess a side wall defined by the buffer material relative to a side wall defined by the dielectric material and relative to a side wall of the at least one trench~~after the oxide layer has been formed~~;

applying ~~a layer of~~ isolation material ~~over said~~ to remaining buffer ~~film layer~~ material, in contact with a portion of the dielectric material exposed laterally adjacent to the side wall of the at least one trench, and filling ~~said~~ the at least one trench;

removing ~~a portion~~ portions of ~~said~~ the isolation material ~~layer above said~~ from the remaining buffer ~~film layer~~material; and

removing ~~said~~ the remaining buffer ~~film layer~~material to exposed side walls of at least one isolation structure protruding from the dielectric material and located laterally beyond corresponding side walls of the at least one trench.

2. (Currently amended) The method of claim 1, wherein forming ~~said~~ the oxide ~~layer~~ includes ~~thermal oxidation of said exposed~~ thermally oxidizing portions of ~~said~~ the semiconductor substrate exposed within ~~said~~ the at least one trench.

3. (Canceled)

4. (Currently amended) The method of ~~claim 3~~claim 1, wherein removing the prtion of the ~~selectively etching said~~ buffer ~~film layer portion results in a portion of said~~ material includes reducing a thickness of the buffer ~~film layer~~ material remaining on ~~said semiconductor substrate and extending a distance from said trench~~the dielectric material.

5. (Currently amended) The method of claim 1, further including annealing ~~said~~ the isolation material, the dielectric material, and the oxide ~~layer~~.

6-10 (Canceled)

11. (Currently amended) A method ~~of~~ for forming a capped shallow trench isolation structure for a semiconductor device, comprising:

~~providing a layered structure comprising~~ applying a dielectric material to a semiconductor substrate;

applying ~~, a dielectric layer, and a~~ buffer ~~film layer~~material to the dielectric material;

etching ~~said layered structure~~ through ~~said~~ the buffer ~~film layer~~material, through ~~said~~ the dielectric ~~layer~~material, and into ~~said~~ the semiconductor substrate to define ~~a~~ at least one trench in the semiconductor substrate without substantially recessing the dielectric material relative to the buffer material~~having sidewalls and a bottom~~;

forming an oxide ~~layer~~ on ~~exposed portions of said~~ side walls and a bottom of the at least one trench in the semiconductor substrate ~~within said trench sidewalls and said trench bottom~~;

~~selectively etching a portion of said~~ laterally recessing at least one side wall of the buffer ~~film layer~~ material ~~after the oxide layer has been formed~~ to expose portions of an upper surface of ~~said~~ the dielectric ~~layer~~ material adjacent to an upper edge of ~~said~~ the at least one trench;

applying ~~a layer of~~ isolation material ~~over said~~ to the buffer ~~film layer~~material, exposed portions of the upper surface of the dielectric material, and the oxide, the ~~said~~ isolation material ~~also~~ substantially filling ~~said~~ the at least one trench;

removing ~~a portion of said~~ portions of the isolation material layer above ~~said~~ the buffer ~~film layer~~material;

removing remaining ~~said~~ buffer ~~film layer~~material; and

etching ~~said~~ the isolation material to form ~~said~~ a capped shallow trench isolation structure with side walls that are located laterally beyond corresponding side walls of the at least one trench.

12. (Currently amended) The method of claim 11, wherein forming ~~said~~ the oxide ~~layer~~ includes ~~thermal oxidation~~ thermally oxidizing material ~~of said exposed portions~~ of ~~said~~ the semiconductor substrate at the side walls of the at least one ~~within said~~ trench.

13. (Canceled)

14. (Currently amended) The method of ~~claim 13~~claim 11, further comprising reducing a thickness of the ~~wherein selectively etching said~~ buffer ~~film~~ material~~layer portion results in a portion of said buffer film layer remaining on said semiconductor substrate and extending a distance from said trench~~.

15. (Currently amended) The method of claim 11, further ~~including~~ comprising annealing ~~said~~ the isolation material, the dielectric material, and the oxide ~~layer~~.

16. (Currently amended) The method of claim 11, wherein ~~said~~ the capped shallow trench isolation structure includes ledges which extend a distance over ~~said~~ the upper surface of the dielectric material ~~said semiconductor substrate~~ adjacent to the ~~said opposing trench~~ edges of the at least one trench.

17. (Currently amended) The method of claim 16, wherein ~~said~~ the ledges extend about 50 and 150 Å over ~~said~~ the upper surface of ~~said semiconductor substrate between about 50 and 150 Å~~dielectric material.

18-24 (Canceled)

25. (Currently amended) A method ~~of~~ for forming an isolation structure on a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench including at least one continuous side wall extending through ~~said~~ the buffer film layer and ~~said~~ the dielectric layer and into ~~said~~the semiconductor substrate, and an oxide layer located on portions of ~~said~~the semiconductor substrate within ~~said~~the trench, the method comprising:

selectively etching a portion of ~~said~~the buffer film layer;

applying a layer of isolation material over ~~said~~the buffer film layer, ~~said~~the isolation material substantially filling ~~said~~the trench;

removing a portion of ~~said~~the isolation material layer above ~~said~~the buffer film layer; and

removing ~~said~~the buffer film layer.

26. (Currently amended) The method of claim 25, wherein selectively etching ~~said~~the portion of ~~said~~the buffer film layer includes performing ~~said~~the selective etching prior to ~~said~~the applying a layer of isolation material.

27. (Currently amended) The method of claim 26, wherein selectively etching ~~said~~the buffer film layer portion results in a portion of ~~said~~the buffer film layer remaining on ~~said~~the semiconductor substrate and extending a distance from ~~said~~the trench.

28. (Currently amended) The method of claim 25, further including annealing ~~said~~the isolation material layer.

29-32 (Canceled)

33. (Currently amended) A method of forming a capped shallow trench isolation structure for a semiconductor device structure that includes a semiconductor substrate, a dielectric layer, and a buffer film layer, a trench including at least one side wall without recesses extending through ~~said~~the buffer film layer and ~~said~~the dielectric layer and into ~~said~~the semiconductor substrate, and an oxide layer located on portions of ~~said~~the semiconductor substrate within ~~said~~the trench, the method comprising:

selectively etching a portion of ~~said~~the buffer film layer to expose portions of an upper surface of ~~said~~the dielectric layer adjacent an upper edge of ~~said~~the trench;

applying a layer of isolation material over ~~said~~the buffer film layer, ~~said~~the isolation material substantially filling ~~said~~the trench;

removing a portion of ~~said~~the isolation material layer above ~~said~~the buffer film layer;

removing ~~said~~the buffer film layer; and

etching ~~said~~the isolation material to form ~~said~~the capped shallow trench isolation structure.

34. (Currently amended) The method of claim 33, wherein selectively etching ~~said~~the portion of ~~said~~the buffer film layer includes performing ~~said~~the selective etching prior to ~~said~~the applying a layer of isolation material.

35. (Currently amended) The method of claim 34, wherein selectively etching ~~said~~the buffer film layer portion results in a portion of ~~said~~the buffer film layer remaining on ~~said~~the semiconductor substrate and extending a distance from ~~said~~the trench.

36. (Currently amended) The method of claim 33, further including annealing ~~said~~the isolation material layer.

37. (Currently amended) The method of claim 33, wherein ~~said~~the capped shallow trench isolation structure includes ledges which extend a distance over ~~said~~the upper surface of ~~said~~the semiconductor substrate adjacent ~~said~~the opposing trench edges.

38. (Currently amended) The method of claim 37, wherein ~~said~~the ledges extend about 50 Å to about 150 Å over ~~said~~the upper surface of ~~said~~the semiconductor substrate ~~between about 50 and 150A~~.

39-52 (Canceled)